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Signed M Cooke

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11APR03 E799670-1 D02879
P01/7700 0.00-0308396.1

1/77

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1. Your reference — PHGB 030043GBP

2. Patent application number
(The Patent Office will fill in this part) — 0308396.1

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KONINKLIJKE PHILIPS ELECTRONICS N.V.
GROENEWOUDSEWEG 1
5621 BA EINDHOVEN
THE NETHERLANDS

Patents ADP Number (*if you know it*) — 07419294001

If the applicant is a corporate body, give the country/state of its incorporation — THE NETHERLANDS

4. Title of the invention — ACTIVE MATRIX DISPLAY DEVICES

5. Name of your agent (*if you have one*)

"Address for service" in the United Kingdom to which all correspondence should be sent (*including the postcode*)

Philips Intellectual Property & Standards
Cross Oak Lane
Redhill
Surrey RH1 5HA

Patents ADP number (*if you know it*) — 08359655001

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Country	Priority Application number	Date of filing
GB	0301659.9	24-1-03

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing (*day/month/year*)

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Description	20 ✓
Claims(s)	5 ✓
Abstract	1 ✓
Drawings	10 + 10 R

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Request for preliminary examination and search (*Patents Form 9/77*)

Request for substantive examination (*Patents Form 10/77*)

Any other documents (*Please specify*)

11. I/We request the grant of a patent on the basis of this application.

Signature [signature] Date 10/4/03

12. Name and daytime telephone number of person to contact in the United Kingdom 01293 81 5280 P L WILLIAMSON

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DESCRIPTION

ACTIVE MATRIX DISPLAY DEVICES

This invention relates to active matrix display devices, particularly but not exclusively active matrix electroluminescent display devices having thin film switching transistors associated with each pixel.

Matrix display devices employing electroluminescent, light-emitting, display elements are well known. The display elements may comprise organic thin film electroluminescent elements, for example using polymer materials, or else light emitting diodes (LEDs) using traditional III-V semiconductor compounds. Recent developments in organic electroluminescent materials, particularly polymer materials, have demonstrated their ability to be used practically for video display devices. These materials typically comprise one or more layers of a semiconducting conjugated polymer sandwiched between a pair of electrodes, one of which is transparent and the other of which is of a material suitable for injecting holes or electrons into the polymer layer.

The polymer material can be fabricated using a CVD process, or simply by a spin coating technique using a solution of a soluble conjugated polymer. Ink-jet printing may also be used. Organic electroluminescent materials exhibit diode-like I-V properties, so that they are capable of providing both a display function and a switching function, and can therefore be used in passive type displays. Alternatively, these materials may be used for active matrix display devices, with each pixel comprising a display element and a switching device for controlling the current through the display element.

Display devices of this type have current-driven display elements, so that a conventional, analogue drive scheme involves supplying a controllable current to the display element. It is known to provide a current source transistor as part of the pixel configuration, with the gate voltage supplied to the current source transistor determining the current through the display element. A storage capacitor holds the gate voltage after the addressing phase.

turned on, a voltage on the column conductor 6 can pass to the remainder of the pixel. In particular, the address transistor 16 supplies the column conductor voltage to a current source 20, which comprises a drive transistor 22 and a storage capacitor 24. The column voltage is provided to the gate of the drive transistor 22, and the gate is held at this voltage by the storage capacitor 24 even after the row address pulse has ended. The drive transistor 22 draws a current from the power supply line 26.

To date, the majority of active matrix circuits for LED displays have used low temperature polysilicon (LTPS) TFTs. The threshold voltage of these devices is stable in time, but varies from pixel to pixel in a random manner. This leads to unacceptable static noise in the image. Many circuits have been proposed to overcome this problem. In one example, each time the pixel is addressed the pixel circuit measures the threshold voltage of the current-providing TFT to overcome the pixel-to-pixel variations. Circuits of this type are aimed at LTPS TFTs and use p-type devices. Such circuits cannot be fabricated with hydrogenated amorphous silicon (a-Si:H) devices, which is currently restricted to n-type devices.

The use of a-Si:H has however been considered. The variation in threshold voltage is small in amorphous silicon transistors, at least over short ranges over the substrate, but the threshold voltage is very sensitive to voltage stress. Application of the high voltages above threshold needed for the drive transistor causes large changes in threshold voltage, which changes are dependent on the information content of the displayed image. There will therefore be a large difference in the threshold voltage of an amorphous silicon transistor that is always on compared with one that is not. This differential ageing is a serious problem in LED displays driven with amorphous silicon transistors.

Generally, proposed circuits using a-Si:H TFTs use current addressing rather than voltage addressing. Indeed, it has also been recognised that a current-programmed pixel can reduce or eliminate the effect of transistor variations across the substrate. For example, a current-programmed pixel can use a current mirror to sample the gate-source voltage on a sampling

first and second capacitors connected in series between the gate and source or drain of the drive transistor, a data input to the pixel being provided to the junction between the first and second capacitors thereby to charge the second capacitor to a voltage derived from the pixel data voltage, and a voltage derived from the drive transistor threshold voltage being stored on the first capacitor.

This pixel arrangement enables a threshold voltage to be stored on the first capacitor, and this can be done each time the pixel is addressed, thereby compensating for age-related changes in the threshold voltage. Thus, an amorphous silicon circuit is provided that can measure the threshold voltage of the current-providing TFT once per frame time to compensate for the aging effect.

In particular, the pixel layout of the invention can overcome the threshold voltage increase of amorphous silicon TFT, whilst enabling voltage programming of the pixel in a time that is sufficiently short for large high resolution AMOLED displays.

Each pixel may further comprise an input first transistor connected between an input data line and the junction between the first and second capacitors. This first transistor times the application of a data voltage to the pixel, for storage on the second capacitor.

Each pixel may further comprise a second transistor connected between the gate and drain of the drive transistor. This is used to control the supply of current from the drain (which may be connected to a power supply line) to the first capacitor. Thus, by turning on the second transistor, the first capacitor can be charged to the gate-source voltage. The second transistor may be controlled by a first gate control line which is shared between a row of pixels.

In one example, the first and second capacitors are connected in series between the gate and source of the drive transistor. A third transistor is then connected across the terminals of the second capacitor, controlled by a third gate control line which is shared between a row of pixels. The second and third gate control lines comprise a single shared control line.

This may be a common cathode line which is shared between a row of pixels. The ability to change the voltage on this line requires it to be "structured", in particular into separate conductors for separate rows.

In order to avoid the need to provide a structured electrode, and to allow all pixels of the array to share a common display element electrode opposite the drive transistor, each pixel may further comprise a second drive transistor. The second drive transistor may be provided between a power supply line and the first drive transistor, or else between the first drive transistor and the display element. In each case, the second drive transistor provides a way of preventing illumination of the display element during an addressing phase, and without needing to change the voltages on a power supply line or on a common display element terminal.

The display element may comprise an electroluminescent (EL) display element, such as an electrophosphorescent organic electroluminescent display element.

The invention also provides a method of driving an active matrix display device comprising an array of current driven light emitting display pixels, each pixel comprising an display element and an amorphous silicon drive transistor for driving a current through the display element, the method comprising, for each pixel:

driving a current through the drive transistor to ground, and charging a first capacitor to the resulting gate-source voltage;

discharging the first capacitor until the drive transistor turns off, the first capacitor thereby storing a threshold voltage;

charging a second capacitor, in series with the first capacitor between the gate and source or drain of the drive transistor, to a data input voltage; and

using the drive transistor to drive a current through the display element using a gate voltage that is derived from the voltages across the first and second capacitors.

This method measures a drive transistor threshold voltage in each addressing sequence. The method is for an amorphous silicon TFT pixel circuit, particularly with an n-type drive TFT, so that a short pixel programming

Figure 8 shows example component values for the circuit of Figures 3 or 7;

Figure 9 shows a schematic diagram of a third example of pixel layout with threshold voltage compensation of the invention;

Figure 10 is a timing diagram for operation of the pixel layout of Figure 9;

Figure 11 shows a schematic diagram of a fourth example of pixel layout with threshold voltage compensation of the invention;

Figure 12 is a timing diagram for operation of the pixel layout of Figure 11.

Figure 13 shows a schematic diagram of a fifth example of pixel layout with threshold voltage compensation of the invention;

Figure 14 is a timing diagram for a first method of operation of the pixel layout of Figure 13.

Figure 15 is a timing diagram for a second method of operation of the pixel layout of Figure 13.

Figure 16 is a modification to the timing diagram of Figure 15;

Figure 17 shows a schematic diagram of a sixth example of pixel layout with threshold voltage compensation of the invention;

Figure 18 is a timing diagram for a first method of operation of the pixel layout of Figure 17.

Figure 19 is a timing diagram for a second method of operation of the pixel layout of Figure 17; and

Figure 20 is a modification to the timing diagram of Figure 18.

The same reference numerals are used in different figures for the same components, and description of these components will not be repeated.

Figure 3 shows a first pixel arrangement in accordance with the invention. In the preferred embodiments, each pixel has an electroluminescent (EL) display element 2 and an amorphous silicon drive

column conductor, so that a full row of pixels is addressed simultaneously, with rows being addressed in turn, in conventional manner.

The circuit of Figure 3 can be operated in a number of different ways. The basic operation will first be described, and the way this can be extended to provide pipelined addressing is then explained. Pipelined addressing means there is some timing overlap between the control signals of adjacent rows.

Only the drive transistor T_D is used in constant current mode. All other TFTs A_1 to A_4 in the circuit are used as switches that operate on a short duty cycle. Therefore, the threshold voltage drift in these devices is small and does not affect the circuit performance. The timing diagram is shown in Figure 4. The plots A_1 to A_4 represent the gate voltages applied to the respective transistors. Plot "28" represents the voltage applied to cathode line 28, and the clear part of the plot "DATA" represents the timing of the data signal on the data line 32. The hatched area represents the time when data is not present on the data line 32. It will become apparent from the description below that data for other rows of pixels can be applied during this time so that data is almost continuously applied to the data line 32, giving a pipelined operation.

The circuit operation is to store the threshold voltage of the drive transistor T_D on C_1, and then store the data voltage on C_2 so that the gate-source of T_D is the data voltage plus the threshold voltage.

The circuit operation comprises the following steps.

The cathode (line 28) for the pixels in one row of the display is brought to a voltage sufficient to keep the LED reversed bias throughout the addressing sequence. This is the positive pulse in the plot "28" in Figure 4.

Address lines A_2 and A_3 go high to turn on the relevant TFTs. This shorts out capacitor C_2 and connects one side of capacitor C_1 to the power line and the other to the LED anode.

Address line A_4 then goes high to turn on its TFT. This brings the anode of the LED to ground and creates a large gate-source voltage on the drive TFT T_D. In this way C_1 is charged, but not C_2 as this remains short circuited.

In the method of Figures 4 and 5, the threshold measurement operation is combined with the display operation, so that the threshold measurement and display is performed for each row of pixels in turn.

Figure 6 shows timing diagrams for a method in which the threshold voltages are measured at the beginning of the frame for all pixels in the display. The plots in Figure 6 correspond to those in Figure 4. The advantage of this approach is that a structured cathode (namely different cathode lines 28 for different rows, as required to implement the method of Figures 4 and 5) is not required, but the disadvantage is that leakage currents may result in some image non-uniformity. The circuit diagram for this method is still Figure 3.

As shown in Figure 6, the signals A_2, A_3, A_4 and the signal for cathode line 28 in Figure 6 are supplied to all pixels in the display in a blanking period to perform the threshold voltage measurement. Signal A_4 is supplied to every pixel simultaneously in the blanking period, so that all the signals A_2 to A_4 are supplied to all rows at the same time. During this time, no data can be provided to the pixels, hence the shaded portion of the data plot at the base of Figure 6.

In the subsequent addressing period, data is supplied separately to each row in turn, as is signal A_1. The sequence of pulses on A_1 in Figure 6 represent pulses for consecutive rows, and each pulse is timed with the application of data to the data lines 32.

The circuit in Figure 3 has large number of rows, for the control of the transistors and for the structure cathode lines (if required). Figure 7 shows a circuit modification which reduces the number of rows required. The timing diagrams show that signals A_2 and A_3 are very similar. Simulations show that A_2 and A_3 can in fact be made the same so that only one address line is required. A further reduction can be made by connecting the ground line associated with the transistor A_4 in Figure 3 to the address line A_4 in a previous row. The circuit in Figure 7 shows the address lines for row n and row n-1.

Figure 8 shows the component values for the circuit of Figure 3 used in an example simulation. The length (L) and width (W) dimensions for the transistors are given in units of μm. The addressing time was 16μs (i.e. the

input voltage is connected directly between the pixel input and the power supply line (to which the transistor drain is connected). The transistor connected to control line A_3, is again for providing a charging path for the first capacitor C_1 which bypasses the second capacitor C_2, so that the capacitor C_1 alone can be used to store a threshold gate-source voltage.

The circuit operation is shown in Figure 10 and has the following steps:

The cathode for the pixels in one row of the display is brought to a voltage sufficient to keep the LED reversed bias throughout the addressing sequence.

Address lines A_2 and A_3 go high to turn on the relevant TFTs, this connects the parallel combination of C_1 and C_2 to the power line.

Address line A_4 then goes high to turn on its TFT, this brings the anode of the LED to ground and creates a large gate-source voltage on the drive TFT T_D.

Address line A_4 then goes low to turn off the TFT and the drive TFT T_D discharges the parallel capacitance $C_1 + C_2$ until it reaches its threshold voltage.

Then A_2 and A_3 are brought low to isolate the measured threshold voltage.

A_1 is then turned on and the data voltage is stored on capacitance C_1.

Finally A_4 goes low followed by the cathode being brought down to ground.

Again, pipelined addressing or threshold measurement in the blanking period can be performed with this circuit, as explained above.

A voltage $V_{data} - V_T$ is thus stored on the gate-drain of the drive TFT. Therefore:

$$I = \frac{\beta}{2}(V_{gs} - V_T)^2 = \frac{\beta}{2}(V_{ds} - V_{dg} - V_T)^2 = \frac{\beta}{2}(V_{ds} - V_{data})^2$$

Hence, the threshold voltage dependence is removed. It is noted that the current is now dependent upon the LED anode voltage.

In the common-cathode circuits of Figures 3, 7 and 9 above, a structured cathode is required to allow the cathodes of individual rows to be switched to different voltages during the addressing cycle.

Figure 13 shows a first modification to the circuit of Figure 3 to avoid the need for a structured cathode. A second drive transistor T_S is provided in series with the first drive transistor T_D, and between the power supply line 26 and the first drive transistor T_D.

In this circuit, a switchable voltage is provided on the power supply line 26 (instead of the cathode line 28), and this is used to switch off the second drive transistor T_S. The timing of operation is shown in Figure 14.

As shown, the operation of the circuit is similar to the operation of the circuit of Figure 4. Instead of the cathode 28 being used to switch off the display element, the power supply line 26 is brought low during the addressing sequence. This turns off the second drive transistor T_S, which is diode-connected with its gate and drain connected together.

The power supply line 26 is high for an initial part of the period when the transistors A_2 –A_4 are turned on, as the power line is used during this time to charge the capacitor C_1 and the second drive transistor T_S needs to be on during this time. This initial period is sufficiently long for the capacitor C_1 to be charged.

When the power supply line is switched low, the second address transistor T_S is turned off. As a result, there is no need to switch off the fourth transistor A_4.

Again, the addressing may be pipelined as shown in Figure 15, in a similar manner as explained with reference to Figure 5.

The addressing scheme of Figure 15 does not allow any duty cycling of the light output. This is a technique by which the drive transistors are not illuminated all of the time. This allows the threshold voltage drift to be reduced, and also allows improved motion portrayal. To provide duty cycle of the drive transistors, the timing operation of Figure 15 is modified as shown in Figure 16.

An example of such a circuit is shown in Figure 17. The gate of the second drive transistor T_S is connected to ground through the fourth transistor A_4, and a fifth transistor A_5 is connected between the gate and drain of the fifth transistor. Otherwise, the circuit is the same as Figure 3 and operates in the same way.

As will be apparent from the following, this circuit avoids the need to provide a switched voltage on either the common cathode terminal of the display elements or on the power supply line.

As shown in Figure 18, the transistors $A_2 - A_5$ are all switched on at the beginning of the addressing phase. As for the circuit of Figure 3, this charges the capacitor C_1 to a level which causes the drive transistor T_D to be turned on, and shorts the capacitor C_2. The source of the drive transistor T_D is connected to ground through the fourth and fifth transistors A_4, A_5. During this time, the second drive transistor T_S is turned off, because the gate is coupled to ground through the fourth transistor A_4.

The gate for the fifth transistor A_5 is then brought low to switch it off. In the same way as for the circuit of Figure 3, the drive current through the drive transistor (because the source-gate voltage has not changed) discharges the capacitor C_1 until the threshold voltage is stored. The voltage on the source of the drive transistor is then the power supply line voltage less the threshold voltage, which is dropped across C_1.

The transistors A_2 and A_3 are then switched off to isolate the capacitors. Before the addressing pulse on A_1, the fifth address transistor is again turned on. This pulls the source of the drive transistor T_D (and therefore one terminal of the data storage capacitor C_2) to ground through the fourth and fifth transistors, so that the data voltage can be stored on C_2 during the addressing phase.

Transistor A_4 is turned off at the end of the addressing pulse in order to allow the second drive transistor T_S to turn on (because its gate is no longer held to ground), and the display element is driven.

Transistor A5 is also turned off at the end of addressing. This maintains a short duty cycle for A5 to prevent significant ageing during operation. The

CLAIMS

1. An active matrix device comprising an array of display pixels, each pixel comprising:

a current driven light emitting display element;

an amorphous silicon drive transistor for driving a current through the display element;

first and second capacitors connected in series between the gate and source or drain of the drive transistor, a data input to the pixel being provided to the junction between the first and second capacitors thereby to charge the second capacitor to a voltage derived from the pixel data voltage, and a voltage derived from the drive transistor threshold voltage being stored on the first capacitor.

2. A device as claimed in claim 1, wherein each pixel further comprises an input first transistor connected between an input data line and the junction between the first and second capacitors.

3. A device as claimed in claim 1 or 2, wherein the drain of the drive transistor is connected to a power supply line.

4. A device as claimed in any preceding claim, wherein each pixel further comprises a second transistor connected between the gate and drain of the drive transistor

5. A device as claimed in claim 4, wherein the second transistor is controlled by a first gate control line which is shared between a row of pixels.

6. A device as claimed in any preceding claim, wherein the first and second capacitors are connected in series between the gate and source of the drive transistor.

16. A device as claimed in claim 15, wherein the ground potential line is shared between a row of pixels and comprises the fourth gate control line for the fourth transistors of an adjacent row of pixels.

17. A device as claimed in claim 1 or 2, wherein the capacitor arrangement is connected between the gate and source of the drive transistor, and the source of the drive transistor is connected to a ground line.

18. A device as claimed in claim 17, wherein the drain of the drive transistor is connected to one terminal of the display element the other terminal of the display element being connected to a power supply line.

19. A device as claimed in claim 17 or 18, wherein each pixel further comprises a second shorting transistor connected across the terminals of the second capacitor.

20. A device as claimed in any one of claims 17 to 19, wherein each pixel further comprises a third transistor connected between the gate and drain of the drive transistor.

21. A device as claimed in claim 20, wherein the third transistor is controlled by a gate control line which is shared between a row of pixels.

22. A device as claimed in any one of claims 17 or 21, wherein each pixel further comprises a fourth charging transistor connected between a power supply line and the drain of the drive transistor.

23. A device as claimed in any one of claims 1 to 16, wherein each pixel further comprises a second drive transistor.

24. A device as claimed in claim 23, wherein the second drive transistor is provided between a power supply line and the first drive transistor.

charging a second capacitor, in series with the first capacitor between the gate and source or drain of the drive transistor, to a data input voltage; and

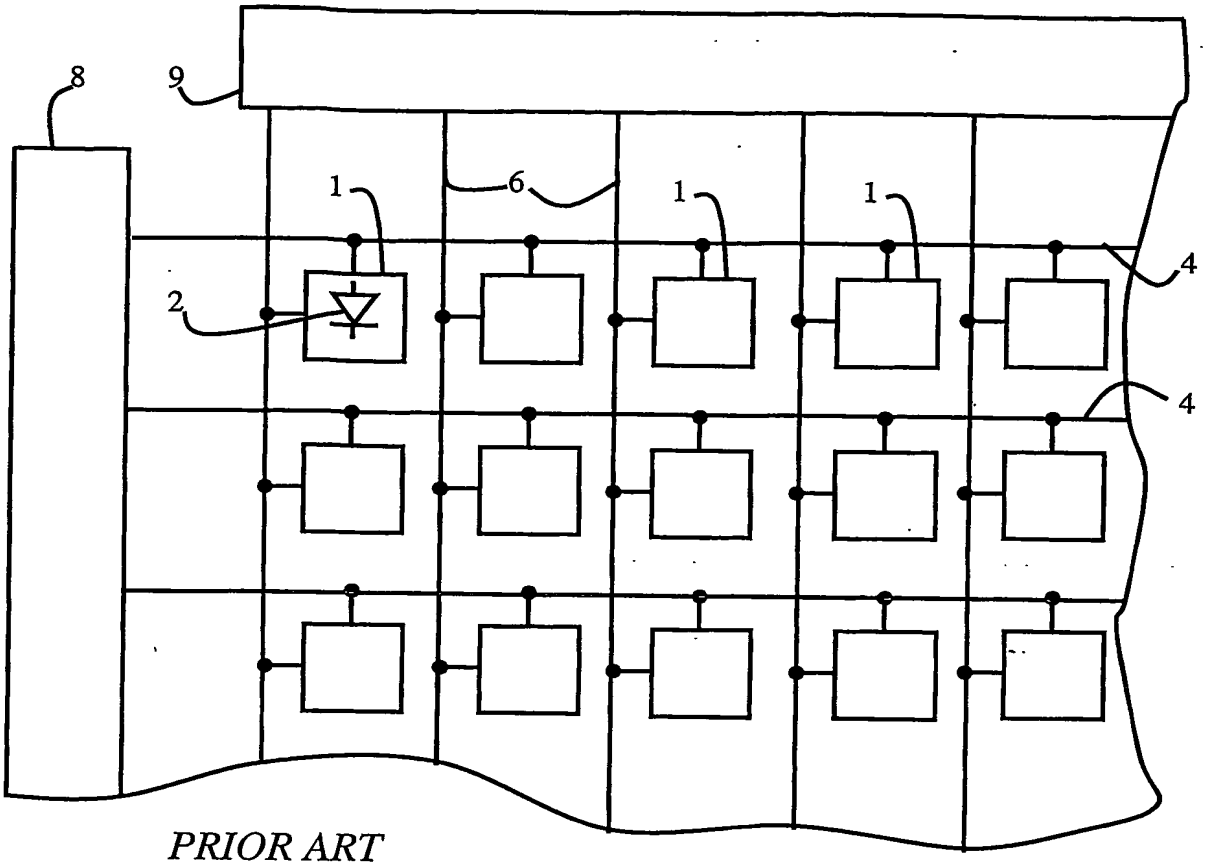
using the drive transistor to drive a current through the display element using a gate voltage that is derived from the voltages across the first and second capacitors.

33. A method as claimed in claim 32, wherein the step of charging a second capacitor is carried out by switching on an address transistor connected between a data line and an input to the pixel.

34. A method as claimed in claim 33, wherein the address transistor for each pixel in a row is switched on simultaneously by a common row address control line.

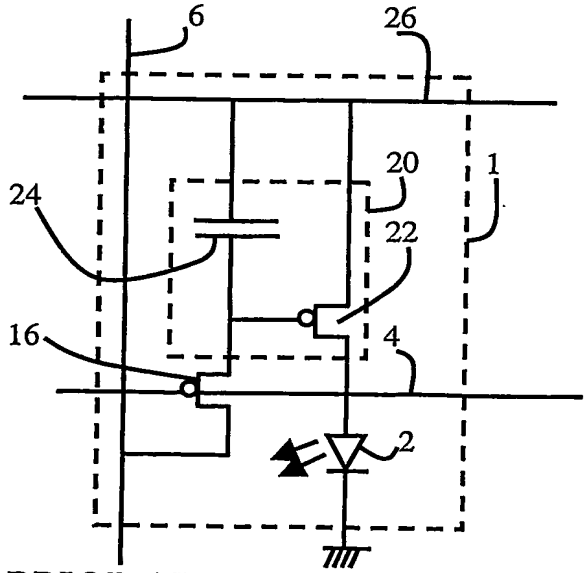
35. A method as claimed in claim 34, wherein the address transistors for one row of pixels are turned on substantially immediately after the address transistors for an adjacent row are turned off.

36. A method as claimed in claim 32, wherein the first capacitor of each pixel is charged to store a respective threshold voltage of the pixel drive transistor at an initial threshold measurement period of a display frame period, a pixel driving period of the frame period following the threshold measurement period.



PRIOR ART

FIG. 1



PRIOR ART

FIG. 2

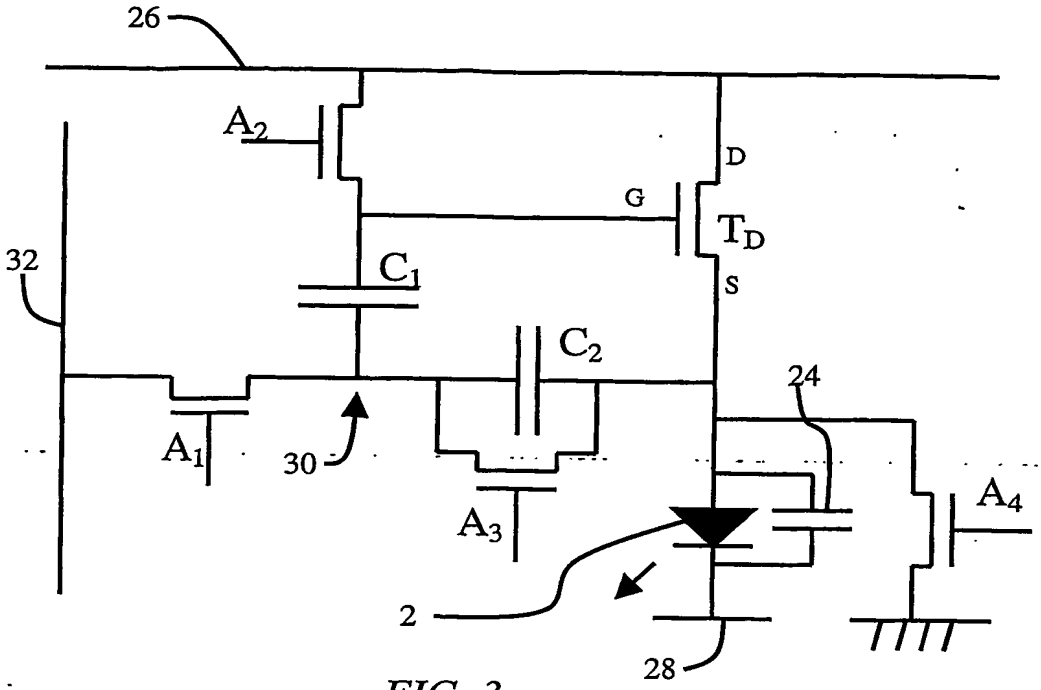


FIG. 3

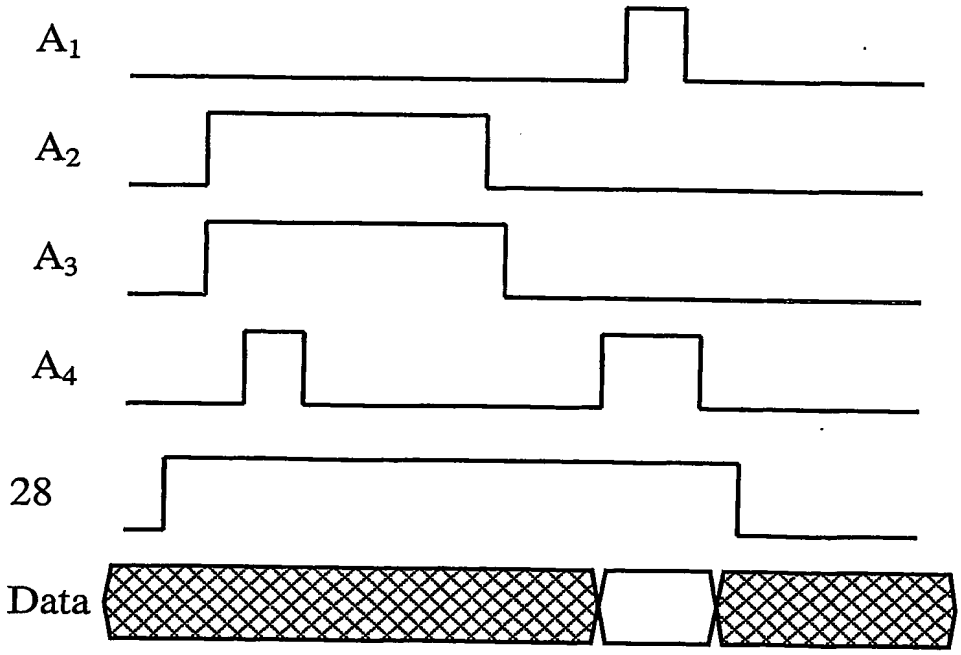


FIG. 4

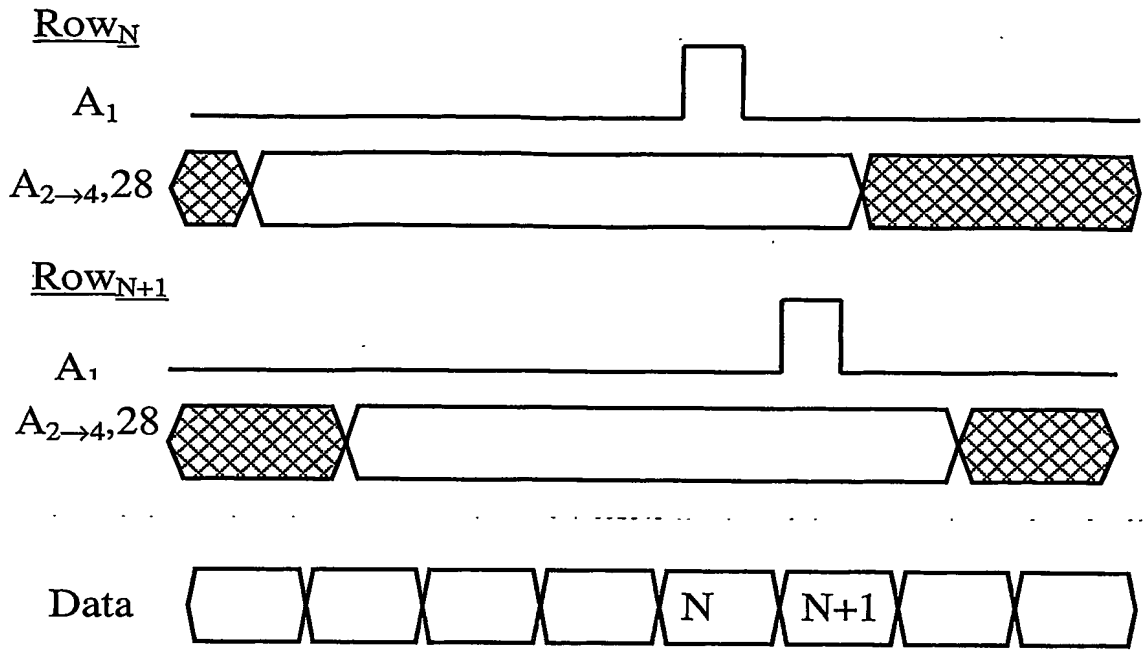

Row$_N$
A_1
$A_{2\rightarrow4}$,28
Row$_{N+1}$
A_1
$A_{2\rightarrow4}$,28
Data
N
N+1

FIG. 5

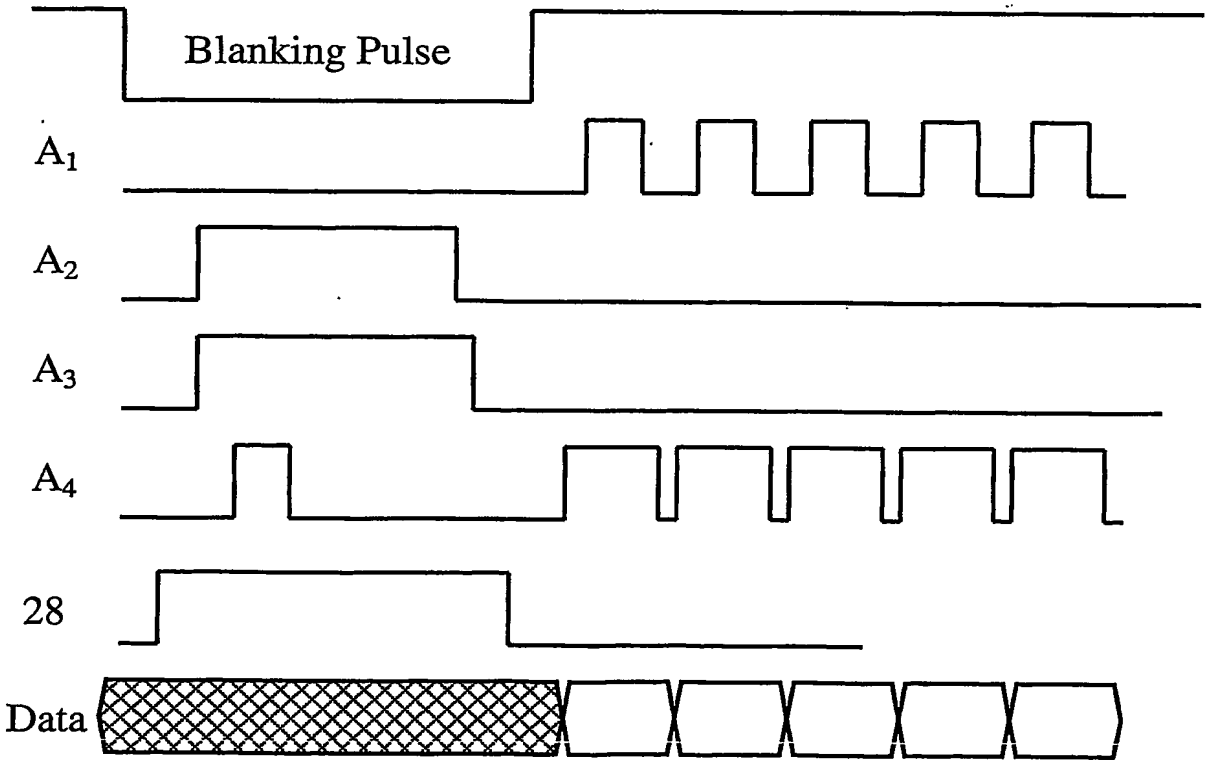

Blanking Pulse
A_1
A_2
A_3
A_4
28
Data

FIG. 6

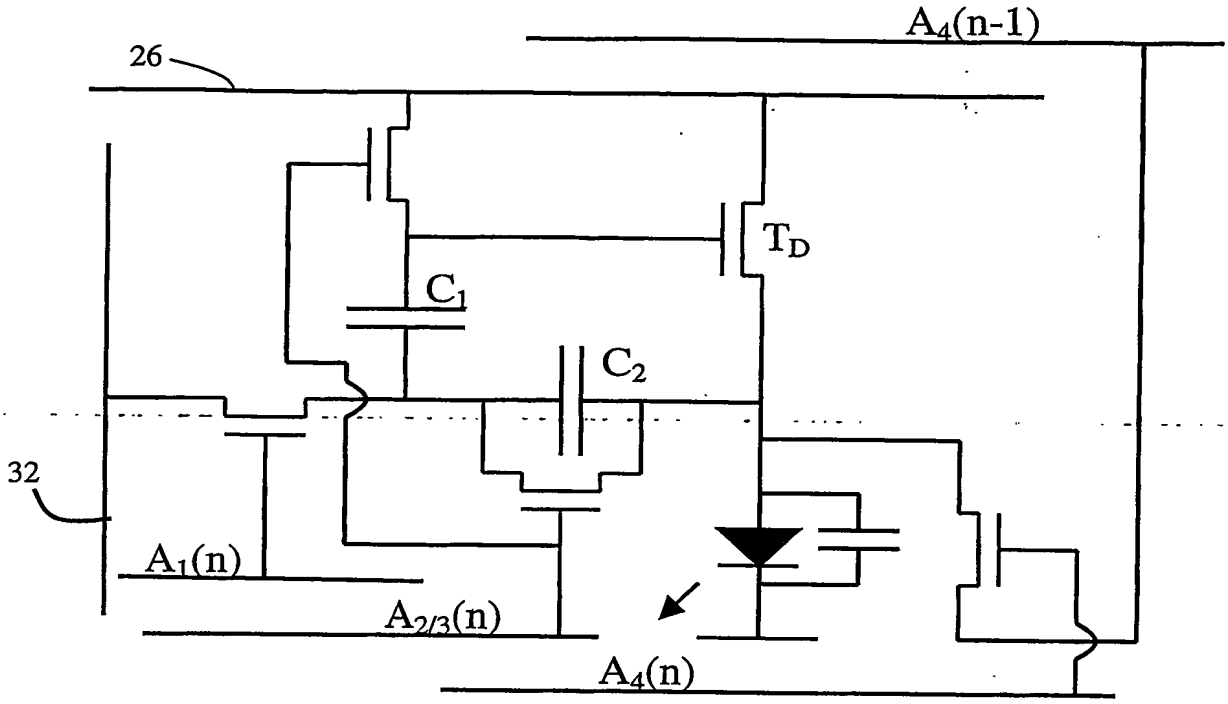

A4(n-1)
26
TD
C1
C2
32
A1(n)
A2/3(n)
A4(n)

FIG. 7

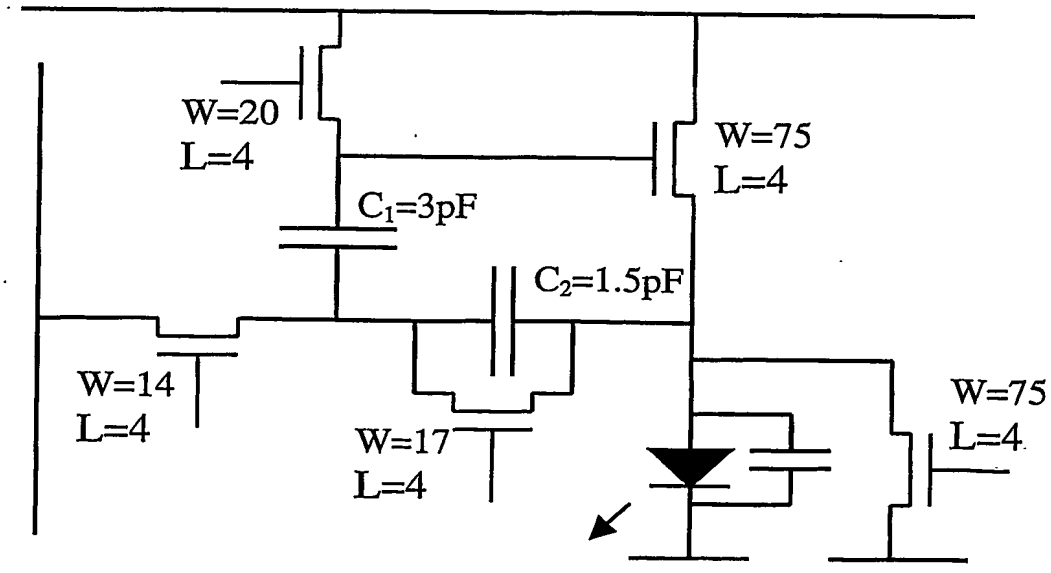

W=20
L=4
W=75
L=4
C1=3pF
C2=1.5pF
W=14
L=4
W=17
L=4
W=75
L=4

FIG. 8

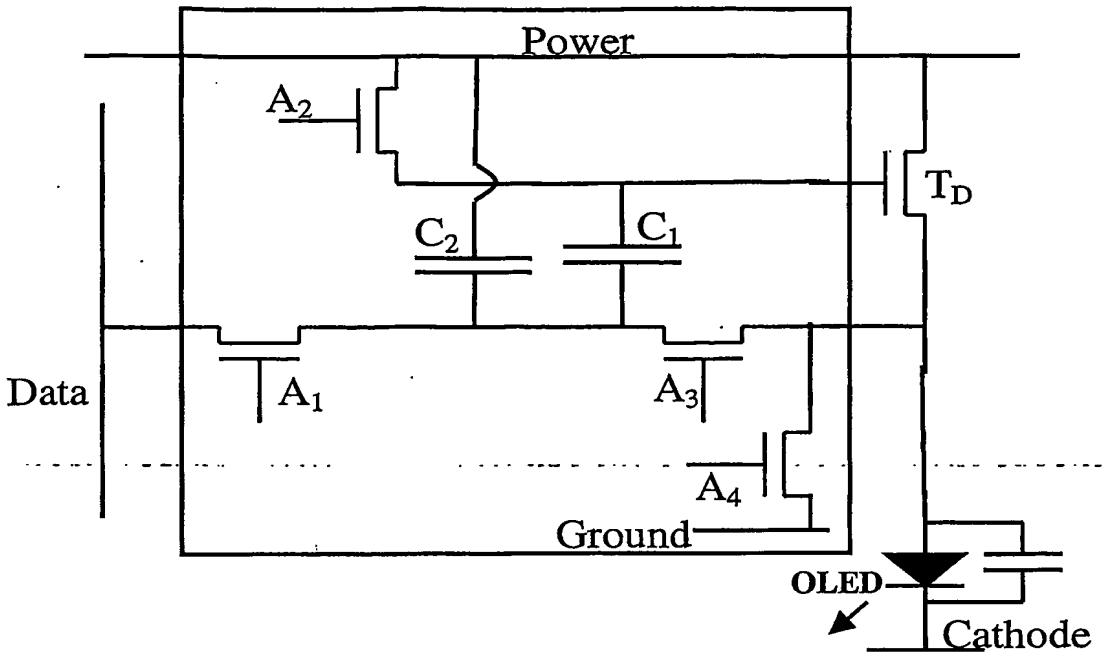

Power
A2
TD
C2
C1
Data
A1
A3
A4
Ground
OLED
Cathode

FIG. 9

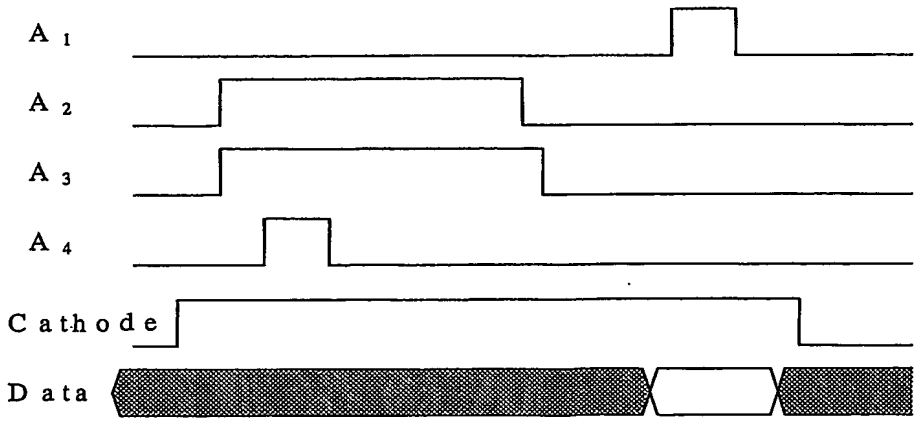

A 1
A 2
A 3
A 4
Cathode
Data

FIG. 10

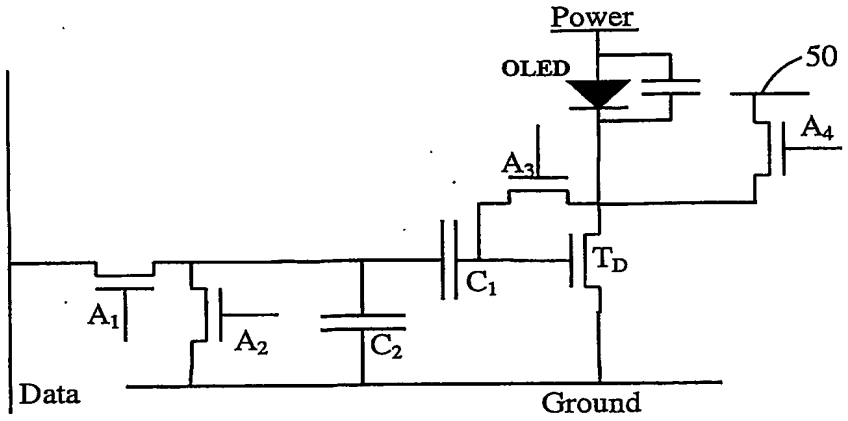

Power
OLED
50
A4
A3
TD
C1
A1
A2
C2
Data
Ground

FIG. 11

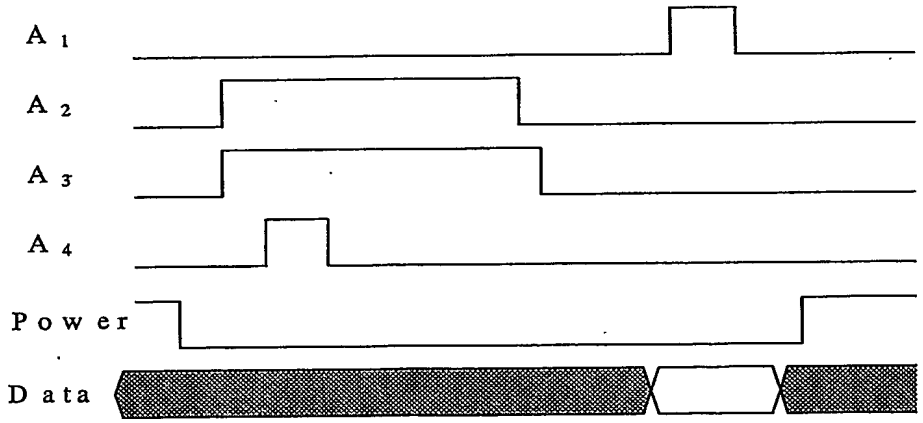

A 1
A 2
A 3
A 4
Power
Data

FIG. 12

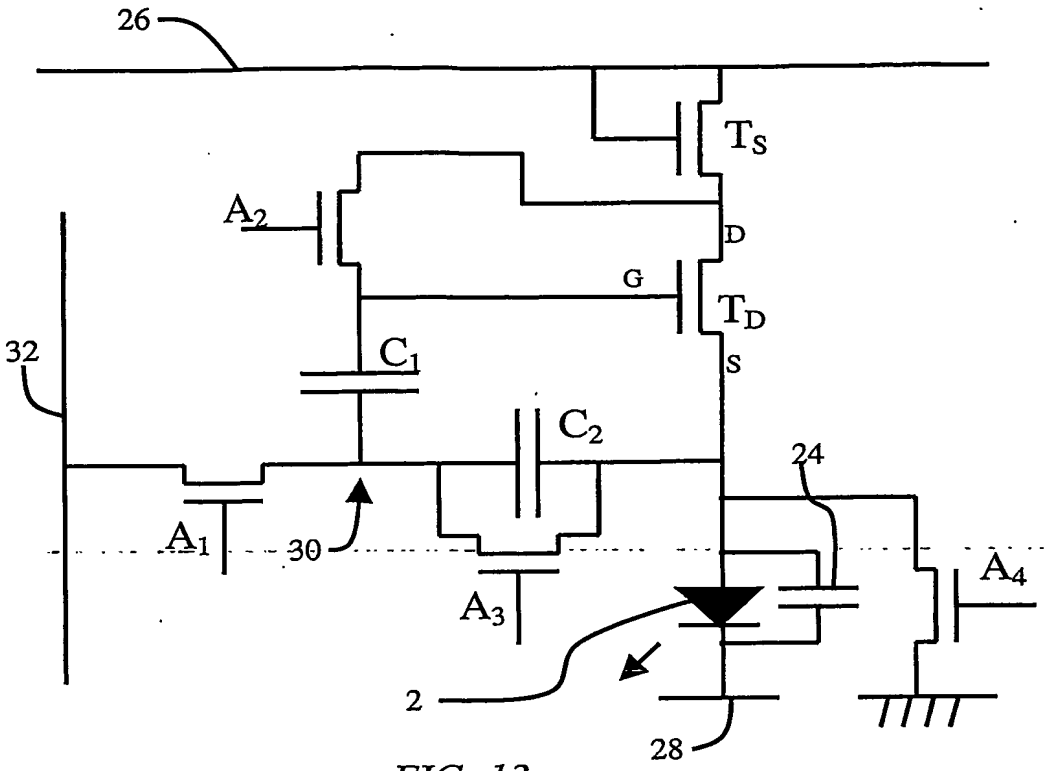


FIG. 13

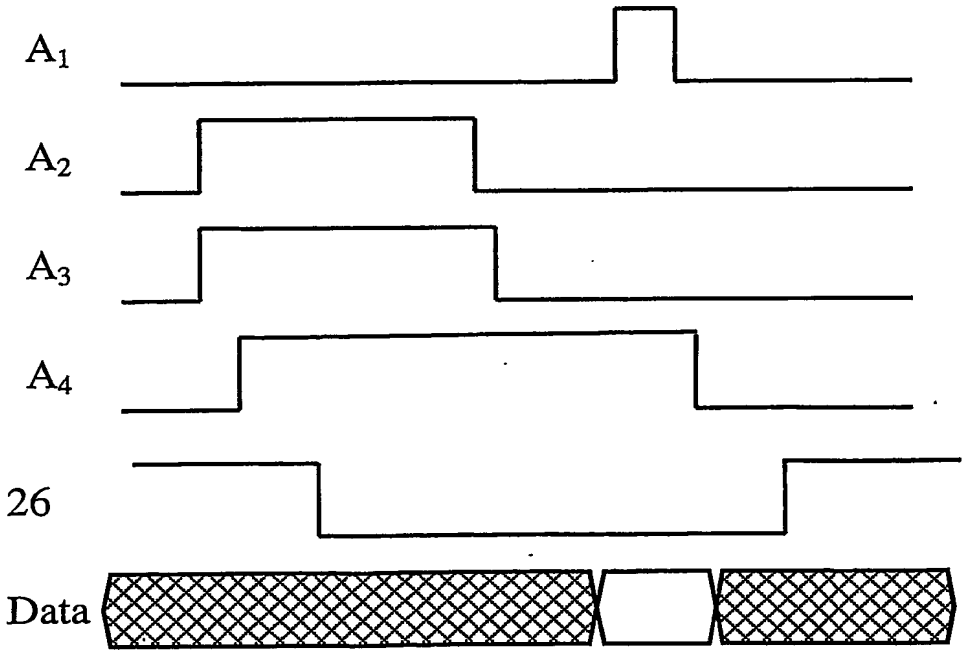


FIG. 14

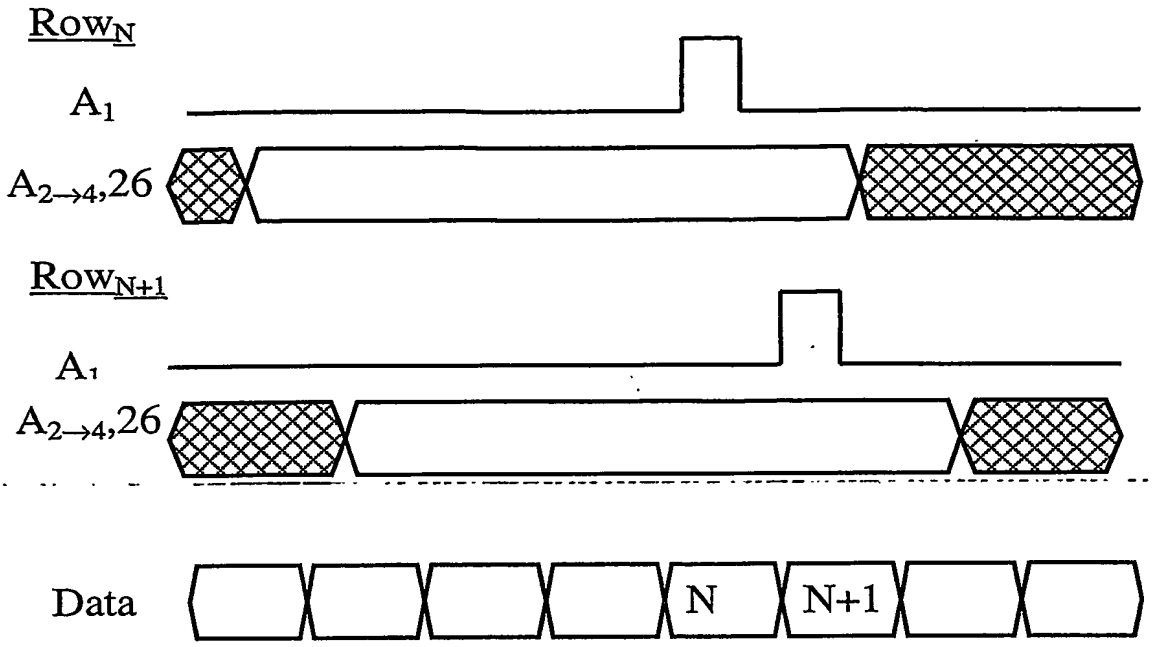

Row_N
A1
A2→4,26
Row_N+1
A1
A2→4,26
Data
N
N+1

FIG. 15

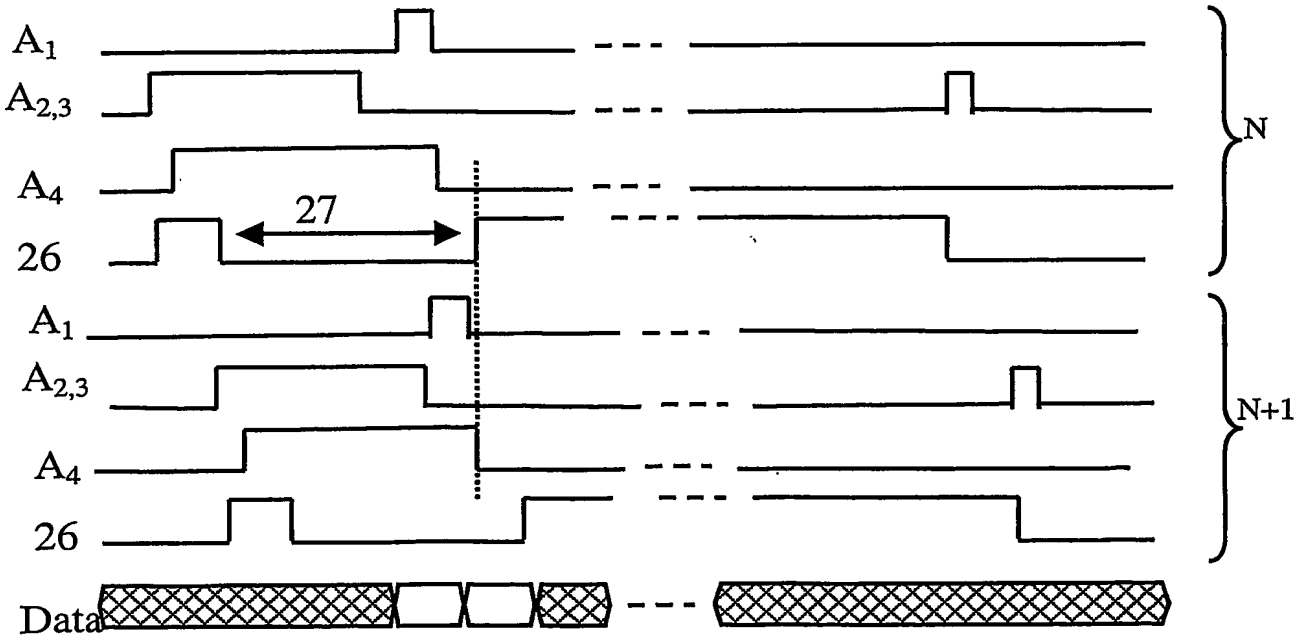

A1
A2,3
A4
26
27
N
A1
A2,3
A4
26
N+1
Data

FIG. 16

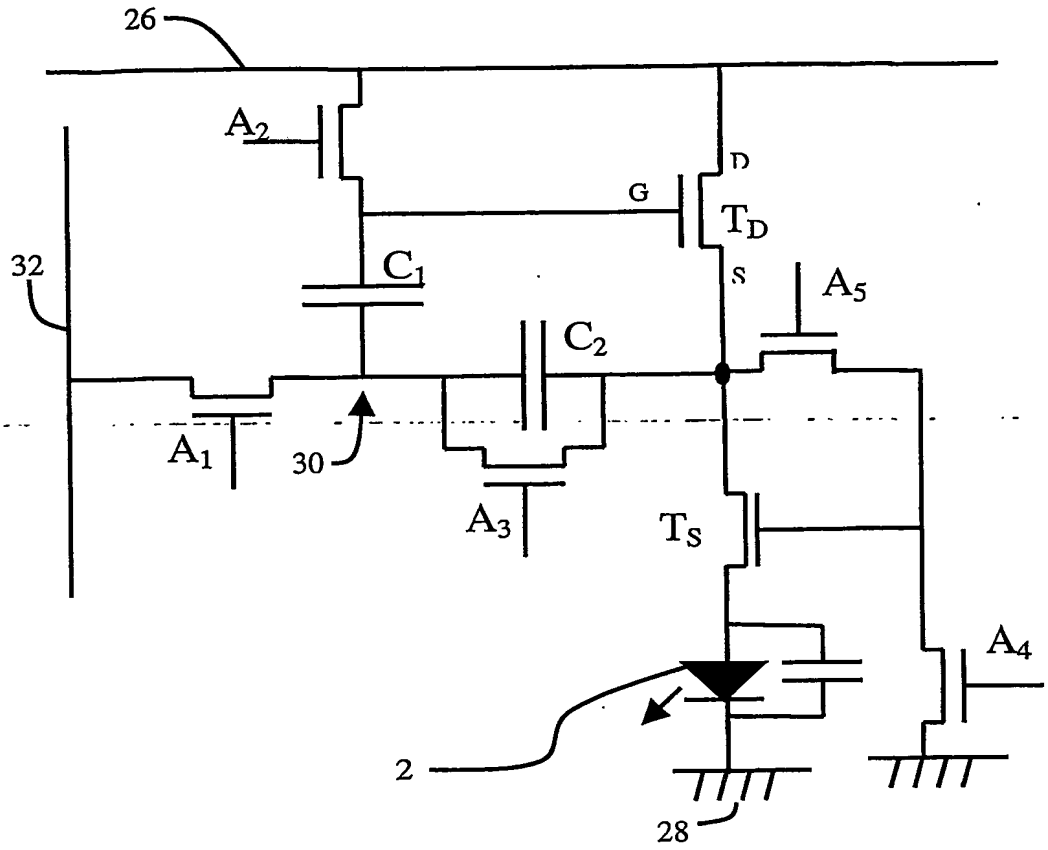


FIG. 17

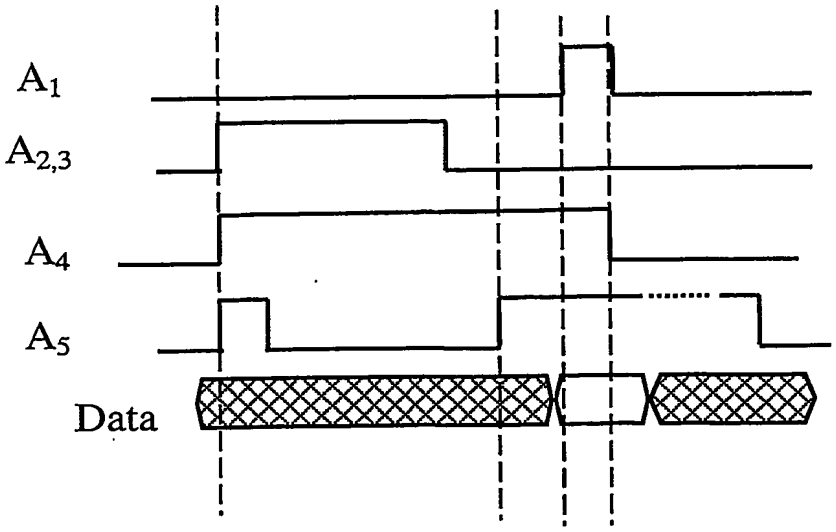


FIG. 18

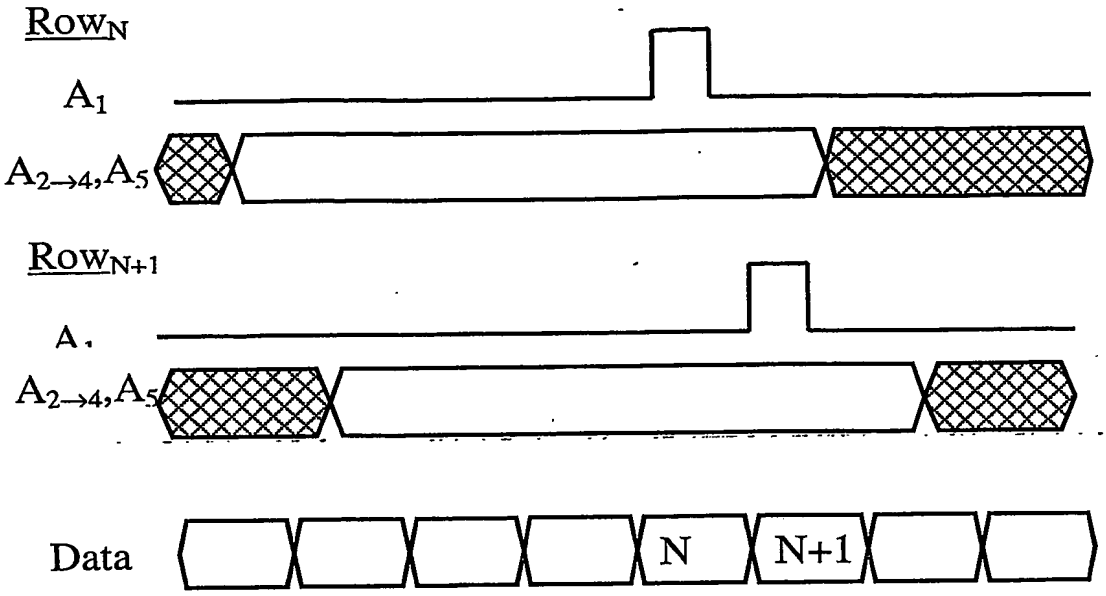

Row$_N$
A_1
$A_{2\rightarrow4}$,A_5
Row$_{N+1}$
A_1
$A_{2\rightarrow4}$,A_5
Data
N
N+1

FIG. 19

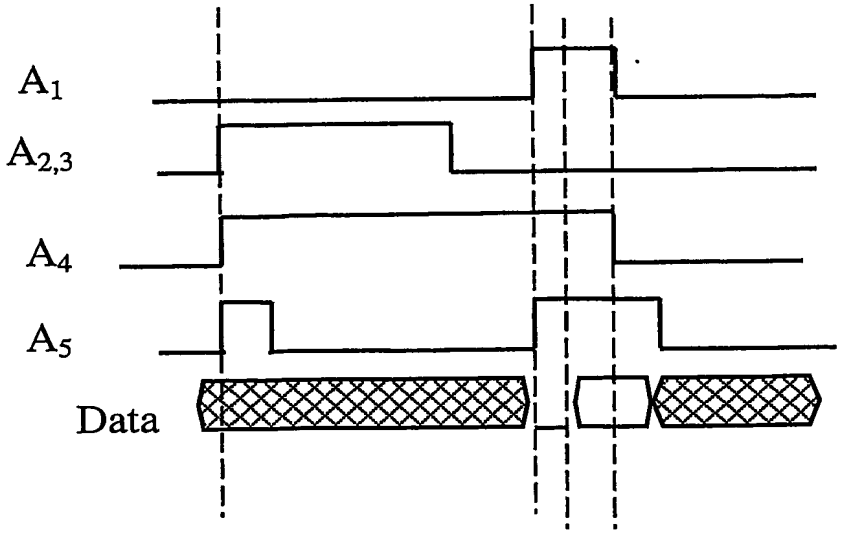

A_1
$A_{2,3}$
A_4
A_5
Data

FIG. 20

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